



1/8

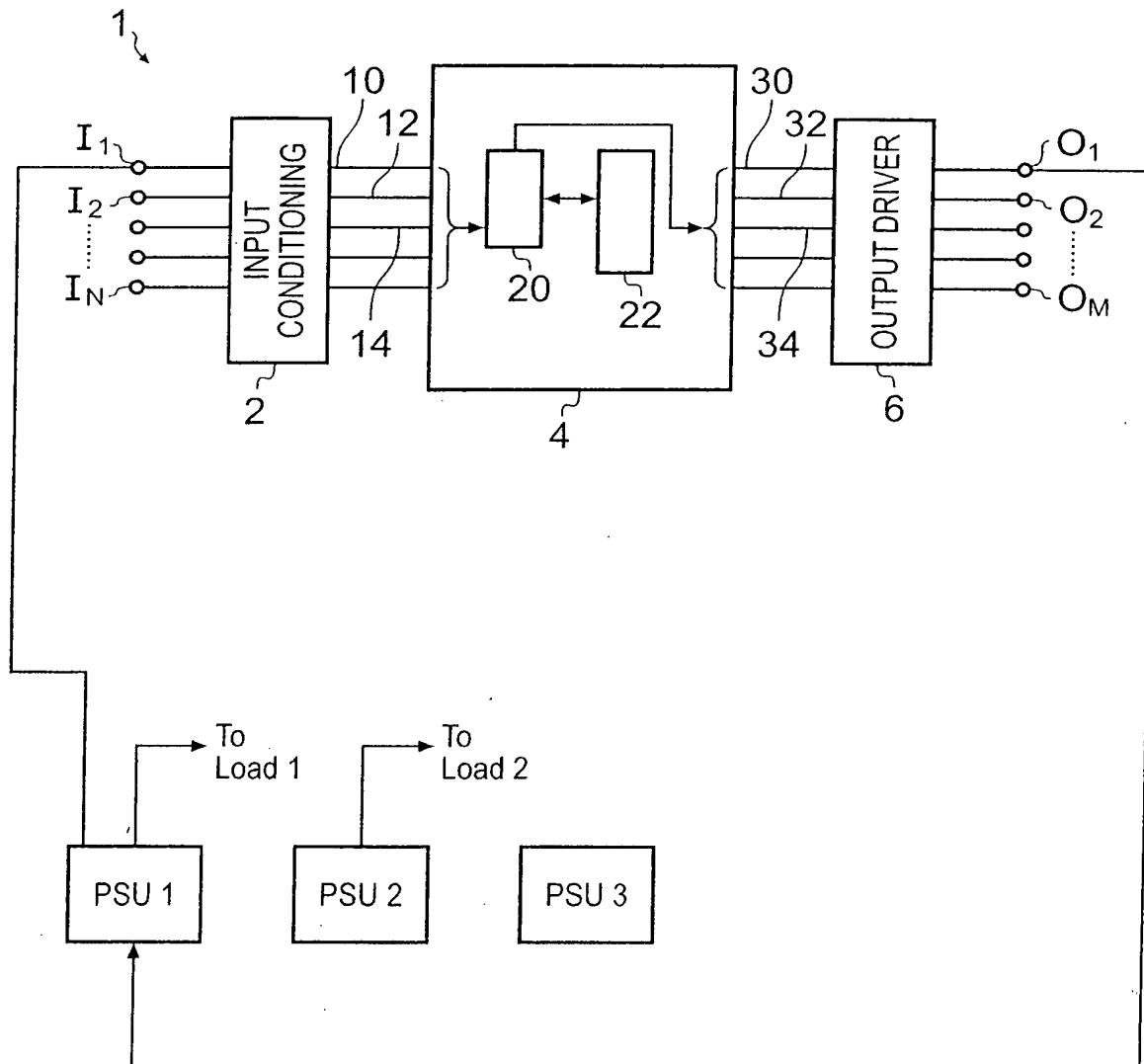


FIG. 1

2/8

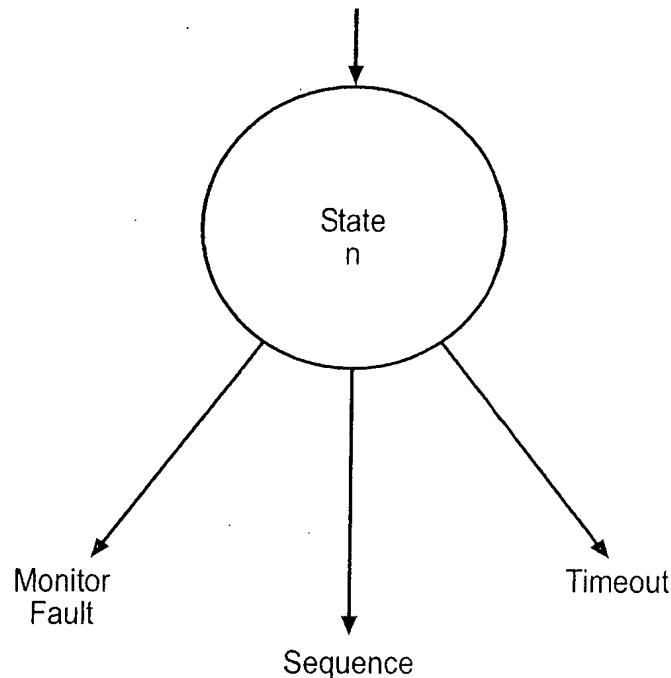


FIG. 2

PDO Outputs	IDLE1	IDLE2	EN3V3	EN2V5	DIS3V3	DIS2V5	PWRGD	FSEL1	FSEL2
PDO1 = 3V3ON	0	0	1	1	0	1	1	1	1
PDO2 = 2V5ON	0	0	0	1	0	0	1	1	1
PDO3 = Fault	0	0	0	0	1	1	0	1	1

FIG. 10

3/8

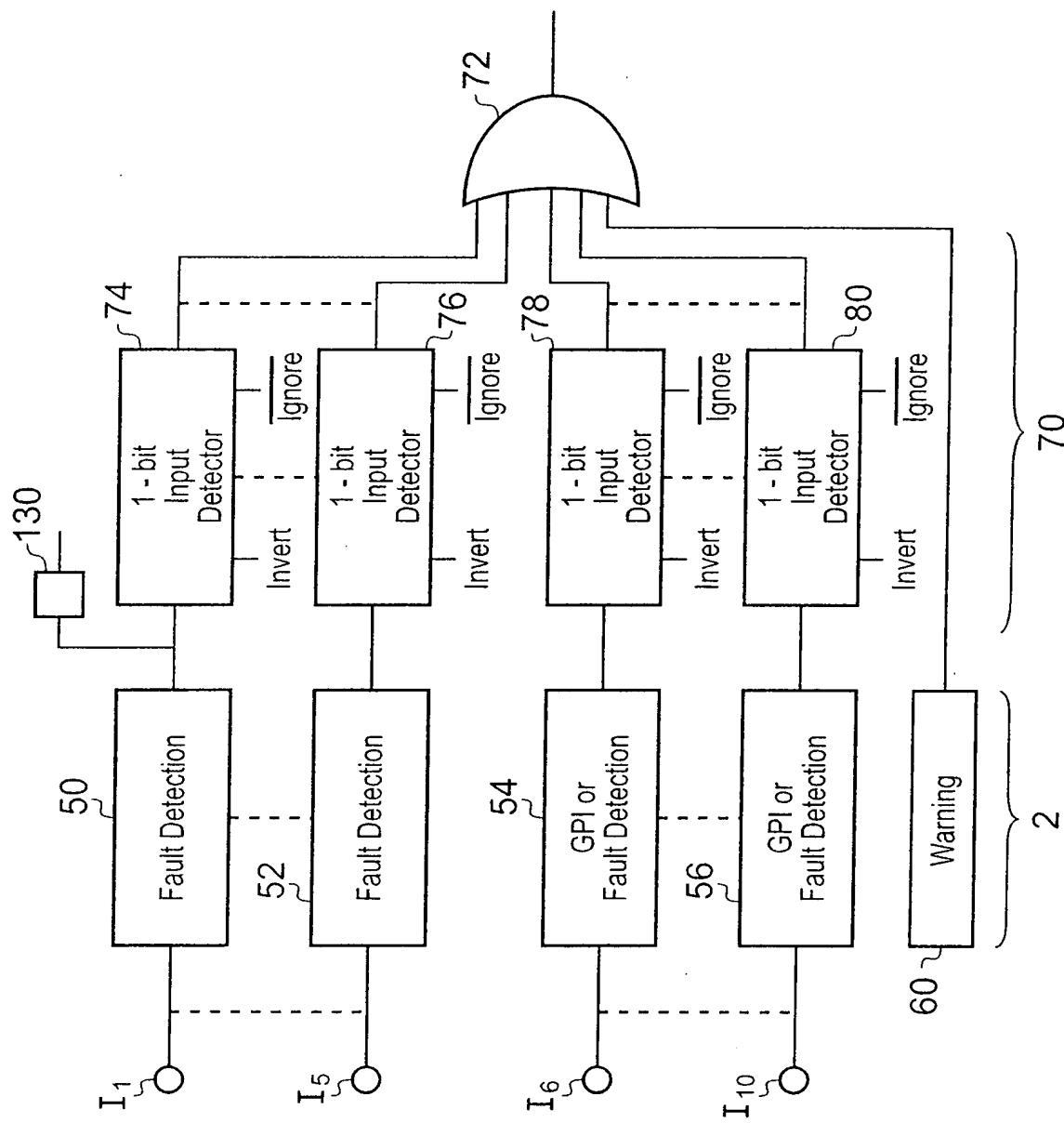


FIG. 3

4/8

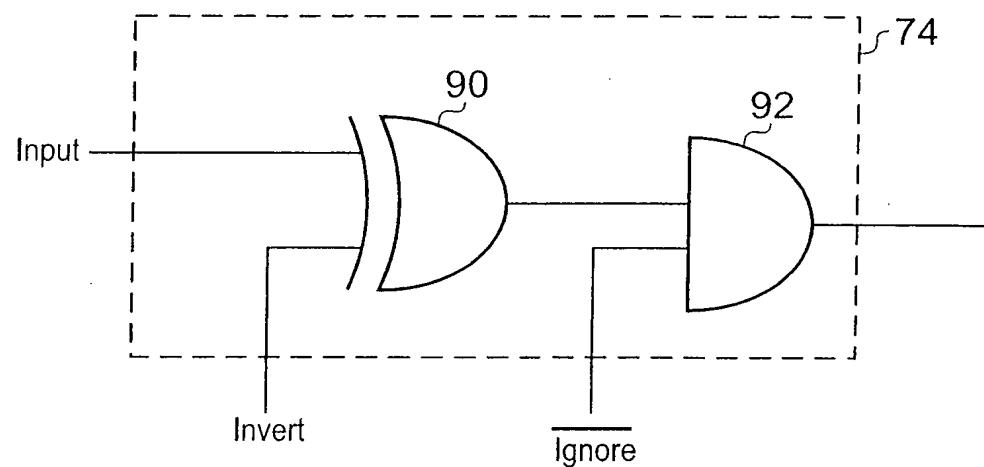


FIG. 4

5/8

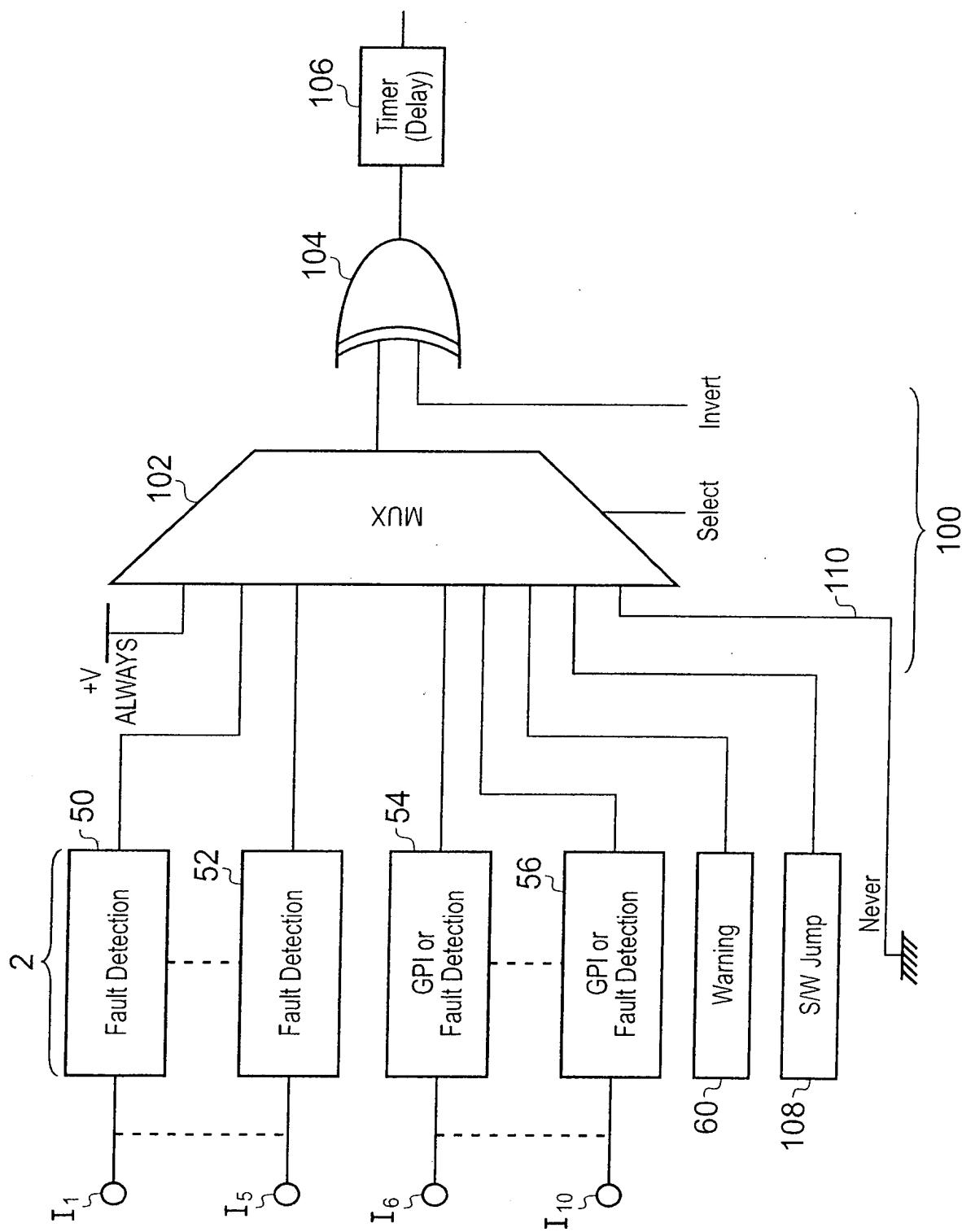


FIG. 5

6/8

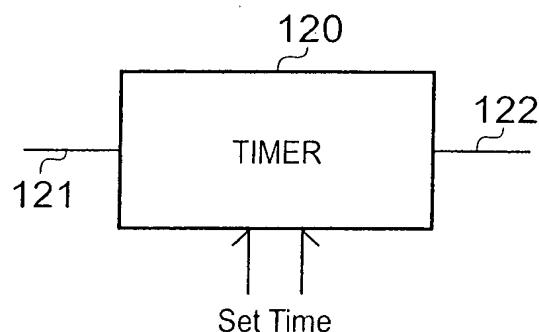


FIG. 6

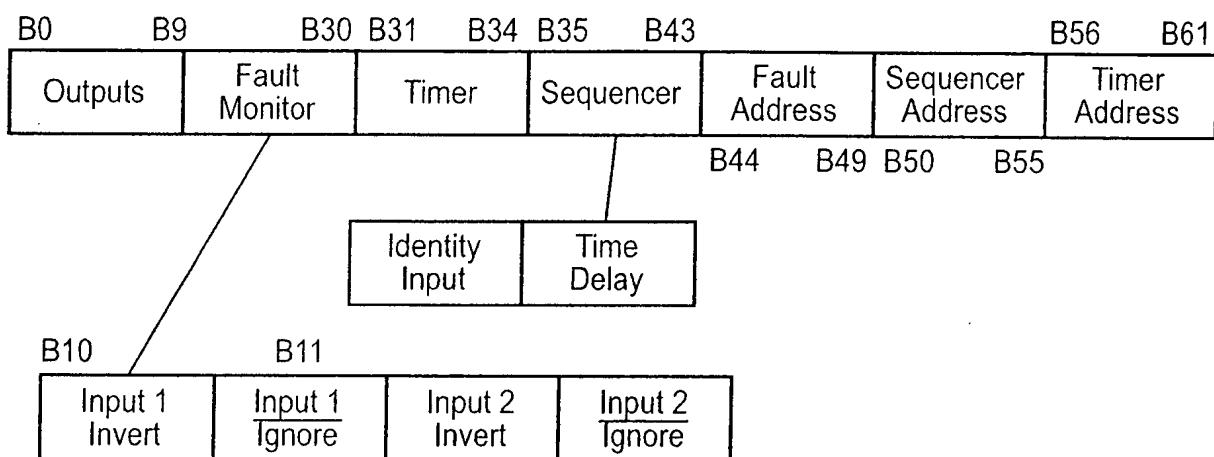


FIG. 7

7/8

State	End of Step	Timeout	Monitor
IDLE1	If VX1 is LOW then goto State IDLE2		
IDLE2	If VP1 is OK then goto State EN3V3		
EN3V3	If VP2 is OK then goto State EN2V5	If VP2 is NOT OK after 10ms then goto State DIS3V3	If VP1 is NOT OK then goto State IDLE1
DIS3V3	If VX1 is HIGH then goto State IDLE1		
EN2V5	If VP3 is OK then goto State PWRGD	If VP3 is NOT OK after 20ms then goto State DIS2V5	If VP1 or VP2 is NOT OK then goto State FSEL2
DIS2V5	If VX1 is HIGH then goto State DIS3V3		
FSEL1	If VP3 is NOT OK then goto State DIS2V5		
FSEL2	If VP2 is NOT OK then goto State DIS3V3		If VP1 is NOT OK then goto State IDLE1
PWRGD	If VX1 is HIGH then goto State DIS2V5		If VP1 or VP2 or VP3 is NOT OK then goto State FSEL1

FIG. 8

8/8

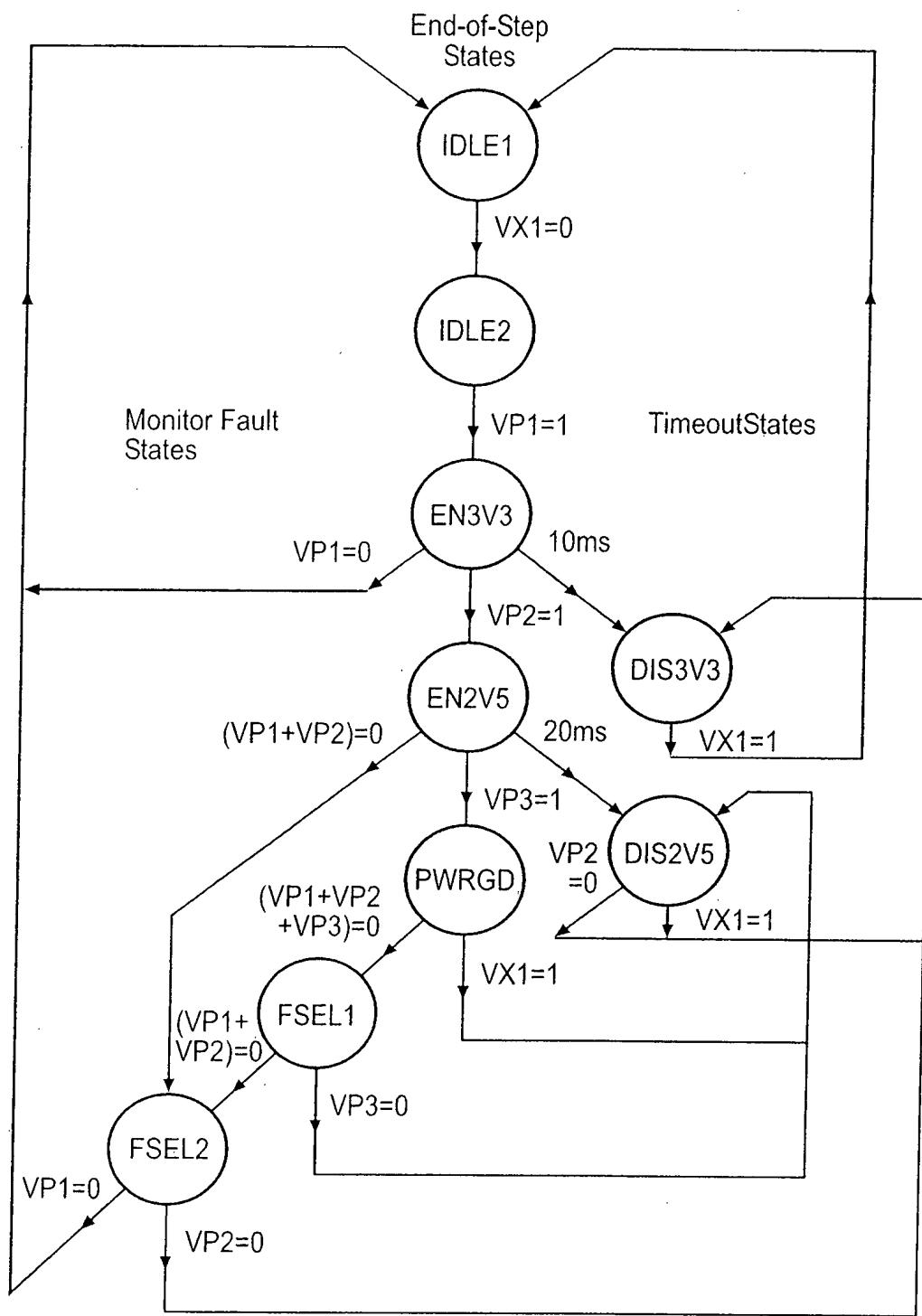


FIG. 9